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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary

Application No.

10/577,017

Applicant(s)

TAKAIKE, EIJI

Examiner

TELLY D. GREEN

Art Unit

2822

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 02 February 2010.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-3, 5-12 and 16-18 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-3, 5-12 and 16-18 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☐ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO/SB-06)
Paper No(s)/Mail Date _____
- 4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date _____
- 5) ☐ Notice of Informal Patent Application
- 6) ☐ Other: _____

DETAILED ACTION

Response to Arguments

Applicant's arguments with respect to claims 1-3, 5-12, 16 and 17 have been considered but are moot in view of the new ground(s) of rejection.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claim 5 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 5 recites the limitation "**the electronic**" in line 2. There is insufficient antecedent basis for this limitation in the claim.

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims **1- 3, 6, 8, 9, 11, 16 and 18** are rejected under 35 U.S.C. 103(a) as being unpatentable over Ahn et al. (Ahn) (**US 2004/0084781 A1**) in view of Anderson et al. (**US Publication 2003/0038415 A1**).

In regards to claims 1, 2 and 16, Ahn (Figs. 1A, 1B and associated text) discloses an electronic element (items 125A, 125B, 125BB, 125N, 125AA, 125NN, 150); and an interposer (items 110 plus 140 plus 145 plus 171 plus 175 plus 155 plus 156 plus 165) including an interposer base (item 110) to which the electronic element (items 125A, 125B, 125BB, 125N, 125AA, 125NN, 150) is joined, and a plurality of post electrodes (items 135) that are disposed inside one or more through holes (portions where items 135 are formed) formed in the interposer base and are connected to corresponding electrodes (item 131) of the electronic element; the interposer base (item 110) comprises a silicon wafer piece (paragraph 26); said interposer (items 110 plus 140 plus 145 plus 171 plus 175 plus 155 plus 156 plus 165) being defined by an upper principal surface (item 115), a lower principal surface (item 120) and a sidewall surface (side surfaces of items 110 plus 140 plus 145 plus 171 plus 175 plus 155 plus 156 plus 165 or 110), said plurality of post electrodes (items 135) extending between said upper principal surface and said lower principal surface of said interposer base so as to penetrate through the silicon wafer piece (item 110), each of said plurality of post electrodes (items 135) having a top end exposed at said upper principal surface, each of said plurality of post electrodes (items 135) having a bottom end exposed as said lower principal surface, said electronic element (items 125A, 125B, 125BB, 125N, 125AA, 125NN, 150) having a top principal surface in indirect contact with said lower principal surface of said interposer, said electronic element (items 125A, 125B, 125BB, 125N, 125AA, 125NN, 150) carrying said plurality of electrodes (items 131) respectively in correspondence to said plurality of post electrodes (items 135), said plurality of electrodes (items 131) being exposed at said top

principal surface of said electronic element (**items 125AA, 125BB, 125NN, 150**) and in contact with corresponding bottom ends of said plurality of post electrodes (**items 135**);

In regards to claims 6, Ahn (Figs. 1A, 1B and associated text) discloses wherein post electrodes (**items 135**) are formed in the single through hole.

In regards to claim 8, Ahn (Figs. 1A, 1B and associated text) discloses a plurality of electronic elements (**items 125A, 125B, 125BB, 125N, 125AA, 125NN, 150**) mounted to the interposer base (**item 110**).

In regards the claim 9, Ahn (Figs. 1A, 1B and associated text) discloses wherein the back surface of the electronic element (**items 125A, 125B, 125 BB, 125N, 125AA, 125NN, 150**) is joined to the interposer base (**item 110**).

In regards to claim 11, Ahn (Figs. 1A, 1B and associated text) discloses wherein the electronic element (**items 125A, 125B, 125BB, 125N, 125AA, 125NN, 150**) is a semiconductor chip (**Abstract, paragraphs 5, 7, 9, 10**).

In regards to claim 18, Ahn (Figs. 1A, 1B and associated text) discloses wherein the portion of the interposer base (**item 131 of item 110**) and the portion of the electronic element (**item 131 of items 125A, 125B, 125BB, 125N, 125AA, 125NN**) that are in direct contact with each other are the same material.

Ahn does not specifically disclose the electronic element and the interposer base are made of the same material.

In regards to claims 1, 2, 3 and 16, Anderson discloses the electronic element and the interposer base are made of silicon/same material (**paragraphs 22, 23**).

Therefore it would have been obvious to one of ordinary skill in the art at the time of the invention to combine the teachings above for the purpose of having a chip and an interposer/interposer base with approximately the same thermal expansion coefficient **(paragraph 23)**.

Claims **5, 7 and 10** are rejected under 35 U.S.C. 103(a) as being unpatentable over Ahn et al. (Ahn) (**US 2004/0084781 A1**) in view of Anderson et al. (**US Publication 2003/0038415 A1**) as applied to claim **1-3, 6, 8, 9, 11, 16 and 18** above and further in view of Yamane et al. (Yamane) (**US Publication 2004/0070064 A1**).

Ahn as modified by Anderson does not specifically disclose wherein the electronic element comprises a first insulating layer formed at least in a position on the electronic element to be joined to the interposer base; and the interposer base comprises a second a second insulating layer; wherein a recess is formed in the interposer base such that the electronic element is accommodated in the recess; a sealing resin encapsulating the electronic element is disposed on the interposer base.

In regards to claim 5, Yamane (Fig. 41 and associated text) discloses wherein the electronic element **(items 20, 48, 10)** comprises a first insulating layer **(item 14)** formed at least in a position on the electronic element to be joined to the interposer base; and the interposer base comprises a second a second insulating layer **(item 24)**.

In regards to claim 7, Yamane discloses wherein a recess is formed in the interposer base such that the electronic element is accommodated in the recess **(Figs. 19I, 19J, 20K-20M)**.

In regards to claim 10, Yamane discloses a sealing resin **(item 40, Fig.41)** encapsulating the electronic element is disposed on the interposer base.

Therefore it would have been obvious to one of ordinary skill in the art at the time of the invention to combine the teachings above for the purpose of protection, thermal expansion coefficient and manufacture cost.

Claim 12 is rejected under 35 U.S.C. 103(a) as being unpatentable over Ahn et al. (Ahn) (**US 2004/0084781 A1**) in view of Anderson et al. (**US Publication 2003/0038415 A1**) as applied to claims 1- 3, 6, 8, 9, 11, 16 and 18 above, and further in view of Terui (**US Publication 2004/0150104 A1**).

In regards to claim 12, Ahn as modified by Anderson does not specifically disclose wherein the electronic element is a passive element.

Terui discloses (**Figs. 4, 6, 12, 16**) wherein the electronic element is a passive element (**paragraph 76**).

Therefore it would have been obvious to one of ordinary skill in the art at the time of the invention to combine the teachings above for the purpose of regulating electrical characteristics (**paragraph 19**).

Claim 17 is rejected under 35 U.S.C. 103(a) as being unpatentable over Ahn et al. (Ahn) (**US 2004/0084781 A1**) in view of Anderson et al. (**US Publication 2003/0038415 A1**) as applied to claim 16 above, and further in view of Chakravorty et al. (Chakravorty) (**US Publication 2003/0185484 A1**).

In regards to claim 17, Yamane as modified by Ahn and Anderson does not specifically disclose wherein the electronic element is an optical device; and the interposer is provided with an optical waveguide optically connected to the optical device.

Chakravorty discloses wherein the electronic element is an optical device; and the interposer is provided with an optical waveguide optically connected to the optical device
(Abstract, paragraphs 11-14).

Therefore it would have been obvious to one of ordinary skill in the art at the time of the invention to combine the teachings above for the purpose of optical and electrical functionality.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire **THREE MONTHS** from the mailing date of this action. In the event a first reply is filed within **TWO MONTHS** of the mailing date of this final action and the advisory action is not mailed until after the end of the **THREE-MONTH** shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than **SIX MONTHS** from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to **TELLY D. GREEN** whose telephone number is (571)270-3204. The examiner can normally be reached on Monday thru Friday 7:30 AM - 5:00 PM EST..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Zandra Smith can be reached on 571-272-2429. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Zandra V. Smith/
Supervisory Patent Examiner, Art
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/Telly D Green/
Examiner, Art Unit 2822
April 23, 2010